REMARKS

The present application was filed on January 5, 2004 with claims 1 through 42. Claims 38-42 were cancelled in the Amendment and Response to Office Action dated December 13, 2005. Claims 1 through 37 are presently pending in the above-identified patent application.

In the Office Action, the Examiner requested that a prior art label be added to Figures 1A-1C, 4A, 4B, 6, and 8. The Examiner rejected claim 12 under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. The Examiner also rejected claims 1-2, 9-10, and 13-15 under 35 USC 102(b) as being anticipated by Mead et al. (United States Patent No. 5,844,265), and rejected claim 11 under 35 U.S.C. §103(a) as being unpatentable over Mead et al., and in view of Ravi et al. (United States Patent Application Publication Number 2004/0263272 A1) and Brachitta et al. (United States Patent Number 6,130,469). Claims 3 and 24 were also rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over claim 1 of United States Patent No. 7,116,594 B2, and claims 4-8, 17-20, 24-28, and 36-37 are rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over claims 1-35 of United States Patent No. 7,116,594 B2. The Examiner indicated that claim 16 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

Formal Objections

Drawings

The Examiner has requested that a prior art label be added to FIGS. 1A-1C, 4A, 4B, 6, and 8. The Examiner asserts that the word "conventional" used in the specification is an adjective to "setting," not to "Field Effect Transistor."

Applicants submit that FIGS. 1A, 1B, 1C, 4A, 4B, 6 and 8 show a gated diode structure with only a gate and a source (and no drain). There are only two terminal areas for the gated diode. The present invention recognizes that this structure (without the drain) leads to a significantly smaller gated diode physical structure (which keeps the area much smaller in applications such as memories and sense amplifiers). Thus, FIGS

1B, 4B, 6 and 8 are different from what is shown by the prior art, including Mead. With regard to the Examiner's references to passages in the specification in the March 1, 2006 Office Action, Applicants respectfully note that the terminology "conventional" on line 10 of page 8 is best understood as modifying "FET", *not* as any admission as to prior art status of material depicted in the pertinent figures; that is, "conventional" FETs can be modified by the teachings of the present invention to obtain the depicted inventive structures. Accordingly, Applicants respectfully submit that the substitute formal drawings submitted on Dec. 13, 2005 have already responded to the Examiner's objection as to FIGS. 2B, 5B, 7 and 9, and that the objection as to FIGS. 1A, 1B, 1C, 4A, 4B, 6 and 8 is inappropriate for the reasons set forth herein.

Applicants respectfully request that the objections to the drawings be withdrawn.

Double-Patenting Rejection

Claims 3 and 24 are rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over claim 1 of United States Patent No. 7,116,594 B2, and claims 4-8, 17-20, 24-28, and 36-37 are rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over claims 1-35 of United States Patent No. 7,116,594 B2.

Applicants are submitting herewith a Terminal Disclaimer to obviate the cited double-patenting rejection. Applicants respectfully request that the double-patenting rejection be withdrawn.

Section 112 Rejections

Claim 12 is rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Regarding claim 12, the Examiner asserts that the cited gated diode is actually a one-terminal device because the source/drain and gate are short-circuited. The Examiner further asserts that there is a contradiction between the recited "two terminal" nature of the claimed "semiconductor device" and the short-circuiting of all terminal(s) of a FET.

Applicants note that the cited claim requires wherein the two terminal semiconductor device comprises a gated diode comprising an insulator formed between a gate and a well, a source diffusion region abutting and overlapping one side of the insulator and gate, a drain diffusion region abutting and overlapping another side of the insulator and gate, and a coupling that electronically couples the source and drain regions, wherein the second terminal is coupled to the source diffusion region and the first terminal is coupled to the gate. Applicants also note that "abutting" is defined as "to be adjacent to." (See, dictionary.com.) Applicants find *no requirement* in claim 12 that the source/drain and gate are short-circuited.

Applicants therefore respectfully request that the section 112 rejection be withdrawn.

Prior Art Rejections

Claims 1-2, 9-10, and 13-15 were rejected under 35 USC 102(b) as being anticipated by Mead et al., and claim 11 was rejected under 35 U.S.C. §103(a) as being unpatentable over Mead et al., and in view of Ravi et al and Brachitta et al. The Examiner asserts that Mead discloses a circuit 10 for amplifying signals, a control line (LOAD BIAS connected to a bias voltage source); and a two terminal semiconductor device 62-1 (MOS transistor used as varactor with source and drain short-circuited), having first and second terminals, the first terminal (gate of gated diode 62-2) coupled to a signal line 194-1 (of sense amplifier 10), and the second terminal coupled to the control line (capacitively, through 16-1). The Examiner further asserts that Mead discloses wherein the two-terminal semiconductor device is CAPABLE of amplifying said signal in response to a substantial change in voltage of said control signal. The Examiner asserts that Applicants admit that any amplifying function is inherent as a property of capability of said gated diode. The Examiner asserts that, in reference to the claim language referring to "wherein the two-terminal semiconductor device is adapted to amplify," intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. Finally, the Examiner asserts that

the limitation "adapted" pertains itself to a method of making the device and as such constitutes a product-by-process limitation.

Mead does not teach a varactor utilized for performing amplification.

Initially, it is noted that the varactors (62-n) of Mead are not even used for signal amplification. Rather, Mead teaches that the "(u)se of a varactor structure allows ***compression*** *of the output signal* over a wide dynamic range of input signals" (See, col 3, lines 25-26; emphasis added.) Applicants also note that Mead teaches that

> another object of the present invention is to provide an integrated photosensing imager system including a sense amplifier having low noise, low power dissipation, and a ***compressive input-output characteristic*** such that it will decrease its gain gradually at large inputs rather than clip abruptly and which can fit into the width of a single pixel in a photosensor array.
> (Col. 1, lines 47-53; emphasis added.)

Mead also teaches that

> a balance transistor 30, shown as a P-C-Channel MOS transistor, is connected between input line 18 and output node 28, and has its gate connected to a BAL signal node 31. In addition, as presently preferred, a varactor structure 32 may be connected between the input and output of amplifier 10. Use of a varactor structure *allows* ***compression*** *of the output signal over a wide dynamic range of input signals.*
> (Col. 3, lines 20-26; emphasis added)

Thus, Mead teaches that the varactor ***compresses*** *signals*; Mead does *not* disclose or suggest that the varactor *amplifies signals*.

Mead does not teach a two-terminal device for performing amplification.

The Examiner is asserting that the three terminal MOS transistors 62-1 through 62-4 in FIG. 7 of Mead are two terminal devices, because the source and drain of the transistors 62-n are short circuited. Assuming for the sake of argument that the transistors 62-1 through 62-4 with connected source and drain are two terminal devices, Mead still does not teach at least one a number of other limitations of the independent claims. In particular, the present invention does *not* claim a two-terminal structure <u>*by itself*</u>. Rather, *each independent claim explicitly recites connecting a two-terminal device*

in a certain way to perform signal amplification.

Mead does not teach an amplification control line.

The transistors 62-n of FIG. 7 in Mead, such as transistor 62-1, are connected between a LOAD BIAS (the Examiner is calling this the control line) and first sense line 194-1 (the Examiner is calling this the signal line).

First, the transistors 62-n in FIG. 7 are *not* directly connected to the LOAD BIAS, but rather are connected to the LOAD BIAS via the output signal (not numbered in FIG. 7 of Mead, but numbered as OUT or 28 in FIG. 1 of Mead). It is noted that the LOAD BIAS is a DC voltage to bias the amplifier which comprises the transistors 12, 14 and 16 in FIG. 1 (often referred to as a cascode amplifier), and is *not* a control line as defined in the art, as defined in the context of the present invention, and as would be well understood by a person of ordinary skill in the art. Both independent claims 1 and 21 require that "*the second terminal (is) coupled to the* ***control line***."

Assuming, for the sake of argument, that one even considers the LOAD BIAS as a control line, the varactors (62-n) are *not* coupled to a control line. Indeed, it is coupled or directly connected to the output of the amplifier which is clearly a signal (numbered as OUT or 28 in FIG. 1 of Mead). Further, in column 3, lines 23 - 25 of Mead, it is noted that "... a varactor may be connected between the input and output of amplifier." The input and output of an amplifier are signals, which cannot be considered as a control line, as defined in the context of the present invention.

Applicants also note that Mead teaches that

> the drain of cascode transistor 14 is connected to the drain of load transistor 16. The source of load transistor 16 is connected to ground rail 24 and the gate of load transistor 16 is connected to load bias node 26. *Load bias node 26 is connected to a bias voltage source* ***supplying a load bias voltage well above the threshold voltage*** *of the transistor*. The output node 28 of amplifier 10 is the common connection of the drains of cascode transistor 14 and load transistor 16.
> (Col. 3, lines 10-18; emphasis added.)

Claim 1 requires a *coupling element coupled to the control line and a control signal, wherein said coupling enables said control signal to* ***control an amplification***, and claim 21 requires *wherein the two terminal semiconductor device*

amplifys said signal in response to a substantial change in voltage of said control signal As noted above, Mead does ***not*** disclose or suggest a *coupling element coupled to a control line and a control signal, wherein said coupling enables the control signal to control an amplification,* Mead does ***not*** disclose or suggest that the varactor is *adapted to amplify a signal*, and does ***not*** disclose or suggest a *substantial change in voltage of a control signal*.

Thus, Mead does ***not*** disclose or suggest that "the second terminal (is) coupled to the control line," does ***not*** disclose or suggest a *coupling element coupled to the control line and a control signal, wherein said coupling enables said control signal to control an amplification,* as required by independent claim 1, and does ***not*** disclose or suggest *wherein the two terminal semiconductor device amplifys said signal in response to a substantial change in voltage of said control signal,* as required by independent claim 21.

Regarding the Examiner's assertion that the limitation "adapted" pertains itself to a method of making the device, that said disclosed gated diode "is in itself not adapted while a function is either is there inherently or is not," that "the process of adaptation itself has no patentable weight in the product invention while only the capability of performing an amplification function is of patentable weight, not the amplification process itself, in as far as claim 1 is concerned," and that, in reference to the claim language referring to "wherein the two-terminal semiconductor device is adapted to amplify," intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art, Applicants note that the cited use of the term "adapted" has been deleted from the cited claims.

Regarding the Examiner's assertion that "only the capability of performing an amplification function is of patentable weight, not the amplification process itself, in as far as claim 1 is concerned," Applicants note that the circuit disclosed by Mead is ***not*** *capable of an amplification function since the LOAD BIAS signal is a DC voltage and not a control signal that can control the amplification function*.

Applicants therefore respectfully request that the rejection under section 102 be withdrawn.

Response to Arguments

Regarding the Examiner's assertion that, "while Applicant appears to admit that Mead et al. teach a two-terminal device, applicant does not appear to believe that claim 1 recites a two-terminal device," Applicants note that, contrary to the Examiner's assertion, it was specifically argued that Mead does *not* disclose a two-terminal device, while the present application does not claim a two-terminal structure ***by itself***. (See, page 8, lines 25-32, of the present Appeal Brief.)

The Examiner asserts that applicant's traverse that "each independent claim explicitly recites connecting such two-terminal devices in a certain way to perform signal amplication" does not find support in the claim language, claim 1 reciting only one two-terminal (semiconductor) device. Applicants maintain that the two-terminal device recited in each independent claim is connected to perform signal amplification, as described in the specification at pages 12-20 and in FIGS. 11-13.

Regarding the Examiner's assertion that, "to exert control over the voltage in a portion of an amplifier 10 qualifies as control of said amplifier and hence said amplification when in use," Applicants maintain that, as argued above, the LOAD BIAS signal is *not* a control line as defined in the art, as defined in the context of the present invention, and as would be well understood by a person of ordinary skill in the art. As noted above, the transistors 62-n in FIG. 7 are not directly connected to the LOAD BIAS, but rather are connected to the LOAD BIAS via the output signal (not numbered in FIG. 7 of Mead, but numbered as OUT or 28 in FIG. 1 of Mead). It is noted that the LOAD BIAS is a DC voltage to bias the amplifier which comprises the transistors 12, 14 and 16 in FIG. 1 (often referred to as a cascode amplifier).

The Examiner asserts that applicant's assertion that Mead is not capable of an amplification function since the LOAD BIAS is a DC signal is a matter of intended use at best and that the Examiner cannot find any restriction to DC voltage in the patent

by Mead et al. The Examiner asserts that the LOAD BIAS 26 appears connected to a threshold voltage dependent voltage (col. 3, lines 10-20) and hence the LOAD BIAS must be capable of variation with said threshold voltage.

Applicants note that, in the absence of a teaching to the contrary, a person of ordinary skill in the art would consider the LOAD BIAS signal to be a DC signal. In any case, as argued above, the circuit disclosed by Mead is *not* configured to be an amplifier and is *not* configured to utilize the LOAD BIAS signal as a control for an amplification function.

Conclusion

The rejections of the cited claims under sections 102 and 103 in view of Mead et al., Ravi et al., and Brachitta et al., alone or in any combination, are therefore believed to be improper and should be withdrawn. The remaining rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.

The attention of the Examiner to this matter is appreciated.

Respectfully,

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